CLAIMS

What is claimed is:

1. A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate;

forming an isolation film within said trench;

forming a first gate stack upon said semiconductor substrate having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks.

2. A process of forming a container cell as defined in Claim 1, wherein said etching a container cell etches said semiconductor substrate such that a portion of said container cell extends beneath said first gate stack.

3. A process of forming a container cell as defined in Claim 1, wherein forming a trench comprises spinning on a photoresist, masking, exposing and patterning said photoresist to create a photoresist mask, and anisotropically etching through said photoresist mask.

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4. A process of forming a container cell as defined Claim 1, wherein said isolation film is a TEOS film.

5. A process of forming a container cell as defined Claim 1, wherein said isolation film is a PSG film.

6. A process of forming a container cell as defined Claim 1, wherein said isolation film is a BPSG film.

7. A process of forming a container cell as defined in Claim 1, wherein forming a first gate stack and forming a second gate stack include forming a silicon nitride spacer, respectively, upon said first and said second gate stacks.

8. A process of forming a container cell as defined in Claim 1, wherein etching a container cell is an RIE etch process.

9. A process of forming a container cell as defined in Claim 1, further comprising:

forming a first polycrystalline silicon layer within said container cell;

depositing a cell dielectric upon said first polycrystalline silicon layer; and

depositing a second polycrystalline silicon layer continuously upon said first gate stack, upon said cell dielectric, and upon said second gate stack.

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10. A process of forming a container cell as defined in Claim 9, wherein said first polycrystalline silicon layer is formed by an in-situ doping CVD process.

11. A process of forming a container cell as defined in Claim 9, wherein said second polycrystalline silicon layer is formed by an in-situ doping CVD process.

12. A process of forming a container cell as defined in Claim 1, wherein said isolation film and said semiconductor substrate have an interface below said container cell.

13. A process of forming a container cell as defined in Claim 1, wherein said isolation film and said semiconductor substrate have an interface below said container cell, such that said interface is coplanar with said edge defined by said semiconductor substrate and said isolation film.

14. A process of forming a container cell as defined in Claim 1, wherein said isolation film and said semiconductor substrate have an interface below said container cell, such that said interface is not coplanar with said edge defined by said semiconductor substrate and said isolation film.

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15. A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate;

forming a conformal isolation film within said trench;

forming a first gate stack upon said semiconductor substrate having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film have an interface that extends below said edge into said semiconductor substrate.

16. A process of forming a container cell as defined in Claim 15, wherein said forming an isolation film is performed by forming an oxide film by the decomposition of TEOS.

17. A process of forming a container cell as defined in Claim 15, wherein said container cell is electrically isolated between said isolation film and said semiconductor substrate.

18. A process of forming a container cell as defined in Claim 15, wherein said etching a container cell comprises RIE.

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19. A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate by spinning on a photoresist, masking, exposing and patterning said photoresist to create a photoresist mask, and anisotropically etching through said photoresist mask;

forming a conformal isolation film within said trench by forming an oxide film by deposition;

forming a first gate stack upon said semiconductor substrate having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film form an interface that extends below said container cell into said semiconductor substrate.

20. A process of forming a container cell as defined in Claim 1, wherein said edge and said interface are coplanar.

21. A process of forming a container cell as defined in Claim 1, wherein said edge and said interface are not coplanar.

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22. A process of forming a container cell as defined in Claim 19, further comprising:

forming a first polycrystalline silicon layer within said container cell;

depositing a cell dielectric upon said first polycrystalline silicon layer; and

depositing a second polycrystalline silicon layer continuously upon said first gate stack, upon said cell dielectric, and upon said second gate stack.

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